

Curriculum Vitae

1. Personal Information	
Name	Mutaz A. B. Al-Tarawneh
Nationality	Jordanian
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2. Academic Qualifications				
	University	Year	Country	Major
B.A	Mu'tah University	2005	Jordan	Computer Engineering
M.A	Southern Illinois University	2008	USA	Computer Engineering
Ph.D	Southern Illinois University	2010	USA	Computer Engineering

3. Research and Teaching Interests	
Computer Architecture	
Real-Time/Embedded Systems	
Power-Aware Computing	
Cloud Computing	
Parallel Programming	

4. Articles				
Title	Publication Date	Journal/Conference	Volume	Pages
Improving the Off-chip Bandwidth Utilization in Chip Multiprocessor (CMP) Using Early Write-Back	2013	Journal of Communication and Computer	10(1)	33-41
An Investigation of the Impact of Instruction Cache (I-Cache) Organization on Power-Performance Trade-Offs in the Design of Scalar Processors.	2013	European Journal of Scientific Research	115(1)	7-26
Performance Evaluation of VLIW and Superscalar Processors on DSP and Multimedia Workloads.	2014	Middle-East Journal of Scientific Research	22(11)	1612-1617

Towards An Optimal Multicore Processor Design for Cryptographic Algorithms – A Case Study on RSA.	2014	WSEAS Transactions on Computers	13(1)	54-77
On the Design of Time-Predictable Low-Leakage Cache Memory for Real-Time Embedded Systems.	2015	WSEAS Transactions on Information Science and Applications	12(1)	82-111
Performance Evaluation of Cooperative Versus Receiver Coded Diversity.	2015	WSEAS Transactions on Communications	14(1)	309-324
A CPU-Guided Dynamic Voltage and Frequency Scaling (DVFS) of Off-Chip Buses in Homogenous Multicore Processors.	2015	International Review on Computers and Software	10(7)	735-747